REMARKS

Claims 1-3, 7-18 and new claims 19-20 are pending in the application.

Objections to Drawings

The Applicant acknowledges and agrees that "Figures 1-3 should be designated by a legend such as - Prior art -because only that which is old is illustrated", however Applicant wishes to point out that Figures 2 and 3 already were, at time of filing, designated by the legend "Prior Art". Accordingly, only Figure 1 has been changed to add the legend "Prior Art". Figures 3 and 5 have been corrected, adding enlarged dots according to established convention, to illustrate more clearly that intersecting lines are electrically connected at those points of intersection. No new matters have been added.

Rejections under Section 112, first paragraph

Claims 11, 12, 14-16 and 18 were rejected under 35 U.S.C. 112, first paragraph because they contained claim limitations expressly reciting "master-slave latch circuitry" without "disclosure of how master [latch] controls the slave [latch]". The claim clause "master-slave latch circuitry" is well known to one ordinary skilled in the art and the terminology describes the relationship between a master latch and a slave latch. For example, a "master latch" and "slave latch" is illustrated in Figure 5 arranged in a master-slave configuration:

Figure 3 also shows a variation of a conventional (CMOS) master-slave latch circuit comprising (single-input) master latches 110 & 130 conjoined with respective (and identical) slave latches 120 & 140. The fact that that master latch (e.g., 110) controls the

data to be latched by the slave latch (e.g., 120) is well understood by one ordinary skilled in the art. Therefore, applicant respectfully requests that the Examiner withdraw all the rejections under 35 U.S.C. 122, first paragraph.

Rejections under Section 103(a)

Claims 1-18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kanoh et al. (US 6,806,859) in view of and/or modified by Goto et al. (US Patent Application 2004/019623 A1). Claims 3-15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kanoh in view Goto "and further, in view of Zavracky et al. (US 2002/0030649)".

The Examiner's reconsideration of the rejections is respectfully requested in view of the amendments.

Currently Amended Claims 1-3, 7-18, and new claims 19-20, further define patentable subject matter (e.g., "source driving circuit" and an "article of manufacture") including the novel combination of features of the disclosed multiplexing-latch circuits. Neither Kanoh nor Goto nor Zavracky teaches the features of the claimed multiplexing-latch circuit nor do they teach or suggest the combination of circuit features claimed in Claims 1-3, 7-18, and new claims 19-20.

The exemplary multiplexing-latch circuits MLA1 and MLA2 illustrated in Figure 5 differ significantly and patentably from the combination of distinct latching and multiplexing circuits illustrated in Figure 3. The circuit of Figure 5 is comparable to the circuit of Figure 3 in that both can perform similar functions (e.g., "R or G" latched output from R & G inputs), and thus the circuit of Figure 5 can replace the circuit of

Figure 3 in "source driving circuits" of displays and in other articles of manufacture. However, the novel circuit of Figure 5 implements similar functions (outputs for inputs) using FOUR LESS TRANSISTORS than the prior art circuit of Figure 3. Thus, the circuit of Figure 5 can be implemented on a chip having less area and smaller dimensions than the circuit of Figure 3, and may consume less electrical power during its operation. Similarly, each of multiplexing-latch circuits MLA1 and MLA2 illustrated in Figure 5 contains TWO LESS transistors than its counterpart (including associated transistors of the multiplexers M1 and M2) in Figure 3.

Therefore, each of Currently Amended Claims 1-3, 7-18, and new claims 19-24, distinctly claim subject matter disclosed in the application that has the requisite novelty and usefulness. A claimed feature of the invention that distinctly and definitely distinguishes its various embodiments from the prior art shown in Figure 3 is that a plurality (e.g., TWO) transmission gates (e.g., 221 and 222) are connected (directly) to the input node of the first inverter (e.g., 231) of the first (master) latch (e.g., 210), performing a multiplexing function; whereas in the prior art of Figure 3, a single transmission gate (e.g., 111) is connected to the input node of the first inverter (e.g., 113) of the first (master) latch (e.g., 110) meanwhile in Figure 3 an ADDITIONAL TWO transmission gates (e.g., 151 and 162) are connected to the output node of the fourth inverter (e.g., 124) of the second latch (e.g., 120) to perform a de/multiplexing function.

The claimed features are not disclosed nor rendered obvious by the admitted prior art (APA) nor by any combination of Kanoh and Goto and Zavracky. Thus, it is believed that currently amended independent claims 1, 9 and 18, and the claims dependent

thereupon, are allowable. The Examiner's reconsideration of the rejection of the claims is respectfully requested.

For the forgoing reasons, the application is believed to be in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

Respectfully submitted,

By: _____

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